## BEE 271 Spring 2017 How to use the SignalTap II logic analyzer Nicole Hamilton

SignalTap II is the builtin Quartus logic analyzer for debugging clocked sequential circuits running on the FPGA. It's comprised of a user interface running on the PC for setting it up and viewing captured data plus the logic analyzer itself, which is compiled onto the FPGA along with your design. The logic analyzer captures data on every positive edge of the clock and then, when a trigger condition is met, transfers it to the PC for display.

The example used here is the simple a 32-bit counter included in Simulation.zip, posted to the files area in Canvas. Download and unzip it and open the SimpleCounter.qpf file.

module CounterA(
 input clock, reset,
 input [ 31:0 ] resetValue,
 output reg [ 31:0 ] count = 0 );
 // Synchronous reset (synchronized to the clock)
 always @( posedge clock )
 count <= reset ? resetValue : count + 1;
endmodule</pre>

In this simple wrapper for the DE1-SoC board, the high-order 10 bits of the counter are tied to the LEDs, the reset value is tied to the switches and the reset button to KEY[3].

```
module SimpleCounter(
    input CLOCK_50,
    input [ 3:0 ] KEY,
    output [ 9:0 ] LEDR,
    input [ 9:0 ] SW );
wire reset = ~KEY[ 3 ];
wire [ 31:0 ] count;
assign LEDR = count[ 31:22 ];
CounterA c ( CLOCK_50, reset, { SW, 22'b0 }, count );
```

endmodule

To add SignalTap II to the project, you must first compile it in Quartus or at least run Analysis & Synthesis. (You can do just that single step by double-clicking the blue triangle.)

You must also plug in and power up a DE1-SoC board.

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	> Fitter (Place & Route)	
	> Assembler (Generate programming files)	
	> TimeQuest Timing Analysis	
	> 🕨 EDA Netlist Writer	
	Edit Settings	
	Nrogram Device (Open Programmer)	
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Then, from the Quartus main menu bar, select Tools  $\rightarrow$  SignalTap II Logic Analyzer to start SignalTap.

Tool	s Window Help
	Run Simulation Tool
	Generate Simulator Setup Script for IP
r.	Launch Simulation Library Compiler
₹\$.	Launch Design Space Explorer II
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-	In-System Memory Content Editor
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01	In-System Sources and Probes Editor
	SignalProbe Pins
$\rightarrow$	Programmer
Q	JTAG Chain Debugger
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1	Tcl Scripts
	Customize
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	Install Devices

This will bring up the SignalTap II logic analyzer screen.

If you see this, "No device is selected", it's because you haven't yet plugged in and powered up a DE1-SoC board. Close the SignalTap window, plug in and power up the DE1-SoC and then restart SignalTap.

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This is what you should see.

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Double clicking to add nodes opens the Node Finder. Filter on "SignalTap II: pre-synthesis" nodes (i.e., the names used in your source, before optimization by the compiler), then click List. You should see something like this.

🥠 Node Finder						×
Named: * Options Filter: SignalTap II: pre-synthesis						List Customize
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					Insert	Close

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Expanding the CounterA and the KEY nodes, Ctrl-left-click to select reset, count, resetValue, KEY[3] and SW, then press > to copy them to right hand panel.

Node Finder				
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LOCK_50	PIN_AF14		SounterA:c count	Unassigned
CounterA:c			CounterA:c resetValue	Unassigned
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count[1]~reg0	Unassigned			
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> Count	Unassigned			
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	PIN Y16			
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You should see this result. Press Insert, then Close.

The SignalTap II window should now look like this. Click "..." to add a clock.

SignalTap II Logic Analyze           File         Edit         View         Project         Project	er - C:/Users/Nicole ocessing <u>T</u> ools <u>W</u>	e/Desktop/Simulation /indow <u>H</u> elp	s/SimpleCounte	er.Thursday/Sim	npleCounter	- SimpleCounter - [stp1.stp	]* — Search alter	a.com	×
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In Node Finder, select CLOCK\_50. Signals will be sampled on the rising edge of this clock.

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In the SignalTap II window, right-click and select "Falling Edge" as the trigger condition.

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Your result should look like this.

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File  $\rightarrow$  Save as "SimpleCounter.stp".

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Yes, you do want to add this to your project.



Press the Compile button. This will trigger a complete recompile in Quartus.

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If you get this error complaining about compiling with SignalTap in your project, you will need to enable TalkBack in Quartus.

© 265013 Can't open SignalTap II Logic Analyzer. Verify that the license file exists and is stored in the correct location. If you are using the Quartus Prime Lite Edition software, you must turn on the TalkBack feature to use the SignalTap II Logic Analyzer.

This is buried in Tools  $\rightarrow$  Options  $\rightarrow$  Internet Connectivity from the Quartus main menu bar. Click "TalkBack Options...".

🕥 Options	×
Category:	
<ul> <li>✓ General EDA Tool Options Fonts Headers &amp; Footers Settings</li> <li>✓ Internet Connectivity Notifications Libraries</li> <li>✓ IP Settings IP Catalog Search Location Design Templates License Setup Preferred Text Editor Processing Tooltip Settings</li> <li>✓ Messages Colors Fonts</li> <li>✓ Text Editor Colors Fonts Autocomplete Text</li> </ul>	Internet Connectivity         Web browser         Use custom web browser instead of system default         Path:         Path:         Proxy server         Access the web using a proxy server         Address:         Pgrt:         User name:         Packets the Altera web site for license updates at startup         Check the Altera web site for new Quartus Prime information         Check the Altera web site for new Quartus Prime information         TalkBack Customer Experience Improvement Program         The TalkBack feature allows Altera to receive limited information concerning the compilation of designs, but not the logic in the designs, to assist in understanding how customers use Quartus Prime software features.         Image: I
< >	OK Cancel Help

Enable TalkBack, click OK twice to get back to Quartus, then retry the compile.

Quartus Prime TalkBack	$\times$						
Enable Advanced							
QUARTUS PRIME SOFTWARE - TALKBACK FEATURE	^						
INTRODUCTION							
The TalkBack feature, included with the Licensed Program(s), enables ALTERA to receive limited information concerning the Licensed Program(s) that you use and your compilation of logic designs (but not the logic design files themselves) using the Licensed Program(s). One of the primary purposes of the TalkBack feature is to assist							
Enable sending TalkBack data to Altera							
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After the compile successfully finishes in Quartus, program the DE1-SoC.

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Close and then re-open SignalTap II and click the continuous button.

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It will then switch to acquisition mode.

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-			Image: A start of the start	XXXh		Nadaa Al		
						<		
🥦 Data	🛲 Setup							
	· · ·	1						
Hierarchy L	Display: ×	Data Log: M					X	
	Counter     CounterA:c	auto signa	itap_0					
🛃 auto_s	signaltap_0						0% 00:00:00	

Each time the reset key is pressed, the captured data is displayed. (The hex 3F3 is what happened to be entered on the switches when I pressed reset.)

SignalTap II Logic Analyzer - C:/User <u>File</u> Edit <u>View</u> <u>Project</u> Processing <u>T</u>	s/Nicole/Desktop/Simulations/SimpleCour ools <u>W</u> indow <u>H</u> elp	nter.Thursday/SimpleCounter - SimpleCounter - [SimpleCo	u – 🗆 X
😽 🕄 つ c 🛃			] •
Instance Manager: 📉 😥 🔳 💆 🗛	quisition in progress	× JTAG Chain Configuration: JTA	G ready ×
Instance Status	Enabled LEs: 1275 Memory: 9728	Small: 0/0 Medium: 2/ Hardware: DE SoC (USB 1)	v Satup
auto_signaltap_0 Waiting for t	ri 🗹 1275 cells 9728 bits	0 blocks 2 blocks	Setup
		Device: @2: 5CSE(BA5 MA8	5)/5CSTFD5 🔻 Scan Chain
٢		>> SOF Manager:	
log: Trig @ 2016/10/27 10:35:48 (0:0:5.8 el	apse	click to insert time bar	
Type Alias Name	-3 -2 -1	<u> </u>	4 5,
CounterA:c/reset	Econon		
CounterA:c/count[31.0]	FCC00000		CUUUU3n / FCCUUUU4n /
* KEY[3]		1000000	
		3F3h	
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🔝 auto_signaltap_0			

## Zooming in:

Name	-1 (	ρ <u>1</u>		2		3	4
CounterA:c reset							
	FCC0	0000h X	FCC00001h	X	FCC00002h	X FCC00003h	
E CounterA:c resetValue[310]			FCC00000h				
KEY[3]							
						3F3h	

On the falling edge of reset, as you release the button, it starts counting from the value entered via the switches.

To end the session, press Esc. Occasionally, I find that SignalTap hangs and will not exit. Unplugging the DE1-SoC will get it unstuck.